BUCK/BOOST CONVERTER MODELING AND SIMULATION FOR PERFORMANCE OPTIMIZATION

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ABSTRACT
High efficiency of DC/DC converters is important in many portable applications to extend the available energy cycle of energy sources. Other applications benefit from energy savings. This work offers modeling and simulation techniques to analyze and design for an overall efficiency optimization of standard synchronous and asynchronous buck/boost converter topologies including variable switching frequency loads. Loss equations are developed, modeled, and simulated along with common power electronic components utilizing Matlab/Simulink SimPower toolbox. Optimization curves are developed for various cases and analyzed to aid in design.

KEY WORDS
Power electronic DC/DC converters; buck/boost; optimization; efficiency; loss modeling

1. Introduction

DC/DC converter performance optimization is important to accommodate the growing need for efficiency in portable electronic device battery life and an ever increasing world climate of energy maximization. The efficiency of two buck/boost converter topologies are examined in this work: the basic non-isolated (no transformer) asynchronous and synchronous converters given in Figures 1 and 2, respectively. Existing efficiency work focuses largely on performance of the buck converter [1][2][3][4][8][9]; these studies do not predict the performance herein outlined for the buck/boost, indicating that buck/boost specific studies are warranted. In addition, recent findings by Xiong et. al.

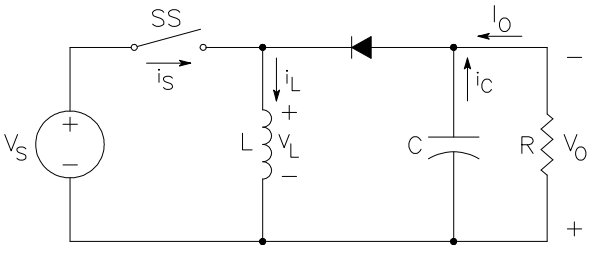

Figure 1. Buck/Boost Converter Architecture (asynchronous)

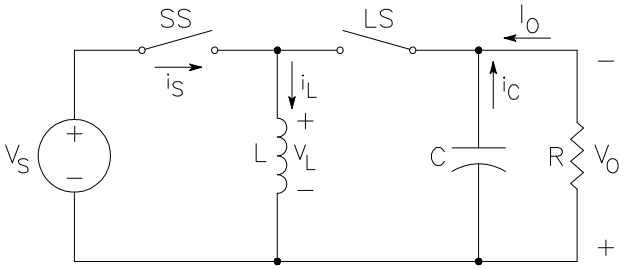

Figure 2. Buck/Boost Converter Architecture (synchronous)

propose that previously accepted methods for calculating MOSFET switching loss have been inaccurate [5], substantiating additional performance optimization analysis and design.

Various techniques exist which improve buck converter performance, including synchronous rectification [2][8], Mode Hopping (CCM/DCM) [9], Zero-Voltage Switching (ZVS) [12][13], variable switching frequency[2][8], and Hybrid (Mode Hopping and variable frequency) [9]. These techniques are summarized and compared by Zhou [1]. Djekic et. al. compared synchronous and asynchronous rectification buck converters for efficiency at various loads and switching frequencies [2]. The work herein accomplishes the same for the buck/boost converter.

The proposed concepts are modeled and simulated via the digital computer utilizing Matlab/Simulink. Section 2 introduces buck/boost converter circuit loss models. Section 3 outlines simulation methodology and study cases. Simulation results are presented in Section 4, followed by a discussion of results in Section 5. Conclusions are stated in Section 6.

Table 1
Buck/Boost Converter Losses Considered

Synchronous	*Asynchronous*
PMOS Conduction	PMOS Conduction
PMOS Switching	PMOS Switching
PMOS Gate Drive	PMOS Gate Drive
NMOS Conduction	Diode Conduction
NMOS Switching	Diode Leakage
NMOS Gate Drive	Diode Junction Capacitance
NMOS Body Diode	
Dead Time	

2. Converter Loss Modeling

Listings of DC/DC converter losses may be found in [1] and [2]. Buck/boost converter losses considered in this work are given in Table 1, as itemized and developed analytically in the following subsections. The designations PMOS and NMOS represent the source switch (SS) and load switch (LS) respectively (reference Figures 1 and 2).

2.1 PMOS Source Switch Conduction Loss

When the PMOS transistor is in forward conduction there is a resistive loss in accordance with eqn.(1),[4],[3]. PMOS conduction loss is associated with both asynchronous and synchronous converters.

$$\text{PMOS Conduction Loss} \triangleq SScL = I_{SS}^2 R_{DS} d \tag{1}$$

where I_{SS}=PMOS current (Amp) R_{DS}=PMOS forward conduction ON resistance (Ohm), d=duty ratio [3],[4]

2.2 PMOS Source Switch Switching Loss

During the transition of voltage rising or falling between the maximum and minimum steady-state value across either switch, and similarly the rise or fall transition of current through the same switch, losses occur. Much work has been performed in an effort to correctly model this behavior [4][5], without a highly accurate model still as yet developed [5]. A combination of the work of [4] and [5] are presented here to develop the switch model beginning with eqn.(2), PMOS switching loss is associated with both converters.

$$P_{SW} = \frac{1}{2} I_{SW} V_{SW} f_s \left(t_{s(off)} + t_{s(on)} \right) \tag{2}$$

where P_{SW}=MOSFET switching loss power (Watt), I_{SW}=current through MOSFET (Amp), V_{SW}=drain to source voltage across MOSFET (Volt), f_s=switching frequency (Hertz), $t_{s(off)}$=MOSFET switching time transitioning off (second), $t_{s(on)}$=MOSFET switching time transitioning on (second) [4],[5]

All parameters of eqn.(2) are readily measurable in a physical circuit except the switching time terms *toff* and *ton* which are developed in the equations that follow.

$$t_{s(on)} = \frac{Q_{G(SW)}}{I_{Driver(L-H)}} \tag{3}$$

$$t_{s(off)} = \frac{Q_{G(SW)}}{I_{Driver(H-L)}} \tag{4}$$

$$I_{Driver(L-H)} = \frac{V_{DD} - V_{SP}}{R_{Driver(Pull-up)} + R_G} \tag{5}$$

$$I_{Driver(H-L)} = \frac{V_{SP}}{R_{Driver(Pull-up)} + R_G} \tag{6}$$

$$V_{SP} \approx V_G + \frac{I_{SW}}{G_m} \tag{7}$$

where $Q_{G(SW)}$=MOSFET switching-point gate charge (Coulomb), $I_{Driver(L-H)}$=MOSFET gate current while switching on (Amp), $I_{Driver(H-L)}$=MOSFET gate current while switching off (Amp), V_{DD}=gate drive controller voltage (Volt), V_{SP}=MOSFET gate voltage at switching point (Volt), $R_{Driver(Pull-up)}$=gate drive controller internal resistance (Ohm), R_G=MOSFET gate resistance (Ohm), V_G=MOSFET gate switching voltage (Volt), G_m=MOSFET transconductance (Siemens) [4],[5]

The traditional method of determining switching-point gate charge value is presented in eqn. (8).

$$Q_{G(SW)} = Q_{GD} + \frac{Q_{GS}}{2} \tag{8}$$

The parameters in (8) are available on MOSFET data sheets. However, Xiong et. al. find this method in determining this value erroneous and present a novel approach in determining switching loss [5]. For the specific transistor used in this work (the IRFP450) the gate charge value of 24nC is used as measured by Xiong et. al. [5].
Combining eqns (3) through (7) gives the combined switching loss *swL* (9).

$$\frac{1}{2} I_{SW} V_{SW} f_s \left(\frac{Q_{G(SW)}}{\dfrac{V_G + \dfrac{I_{SW}}{G_m}}{R_{Driver(Pull-up)} + R_G}} + \frac{Q_{G(SW)}}{\dfrac{V_{DD} - \left(V_G + \dfrac{I_{SW}}{G_m} \right)}{R_{Driver(Pull-up)} + R_G}} \right) \tag{9}$$

2.3 PMOS Source Switch Gate Drive Loss

Gate drive loss accounts for the energy dissipated by the MOSFET to drive the gate for the switching operation. The loss equation is given in eqn. (10). PMOS gate drive loss is associated with both converters.

$$\text{PMOS Gate Drive Loss} \triangleq \text{gdL} = Q_{G(SW)} V_G f_s \tag{10}$$

2.4 NMOS Load Switch Conduction Loss

Load switch conduction loss is similar to that of the source switch shown in eqn. (1), differing by the (1-*d*) factor as this loss occurs during the latter portion of the switching period. This loss is represented in eqn. (11). NMOS conduction loss is associated with only the synchronous converter.

$$\text{NMOS Conduction Loss} \triangleq LScL = I_{LS}^2 R_{DS}(1-d) \quad (11)$$

where I_{LS}=load switch drain to source voltage(Volt)

2.5 NMOS Load Switch Switching Loss

The load switch MOSFET switching loss is calculated with the same model as the source switch shown in (9). NMOS switching loss is associated with only the synchronous converter.

2.6 NMOS Load Switch Gate Drive Loss

NMOS gate drive loss is accounted for by simply doubling the gate drive loss equation (10) for the synchronous case. NMOS gate drive loss is associated with only the synchronous converter.

2.7 NMOS Load Switch Body Diode Loss

The load switch body diode loss occurs only in the load switch due to the reverse bias during the d portion of the period [2]. The reverse-bias voltage and leakage current dissipate power according to the equation shown in eqn. (12). NMOS body diode loss is associated with only the synchronous converter.

$$\text{NMOS Body Diode Loss} \triangleq LSbdL = i_{leakage} V_{LS} d \quad (12)$$

where $i_{leakage}$=reverse bias leakage current (Amp), V_{LS}=load switch drain to source voltage (Volt)

2.8 Synchronous Switching Dead-Time Loss

Dead-time loss occurs through the load switch when neither transistor is on as the load switch is in forward conduction [4]. A period of dead-time must exist to prevent current "shoot-through" whereby current flows through both switches simultaneously to the load. The value of t_{dead} is assumed to be 60ns as is typical for DC/DC converter controllers [2]. The dead-time loss representation is shown in eqn.(13). Synchronous switching dead-time loss is associated with only the synchronous converter.

$$\text{Dead-Time Loss} \triangleq deadL = I_{load} V_{LS} f_s t_{dead} \quad (13)$$

where I_{load}=load current (Amp), t_{dead}=time where both switches are off (second)

2.9 Diode Conduction Loss

Diode forward conduction losses are found with the equation shown in (14). Diode conduction loss is associated with only the asynchronous converter.

$$\text{Diode Conduction Loss} \triangleq DcL = I_D V_f (1-d) \quad (14)$$

where I_D=current through diode (Amp), V_f=diode forward voltage (Volt)

2.10 Diode Reverse Bias Loss

During the portion of the period d, the diode has a reverse bias across it. There is a certain amount of leakage current under this condition that is listed by the manufacturer on the data sheet. This value is used to calculate diode reverse bias leakage loss in eqn. (15). Diode reverse bias loss is associated with only the asynchronous converter.

$$\text{Diode Reverse Bias Loss} \triangleq DrbL = V_D i_{leakage} d \quad (15)$$

where V_D=voltage across diode (Volt)

2.11 Diode Junction Capacitance Loss

Diodes have a certain capacitance associated with changing voltages across them [4]. The charging and discharging of this capacitance creates a power loss as modeled by equation (16). Diode junction capacitance loss is associated with only the asynchronous converter.

$$\text{Diode Capacitive Loss} \triangleq DcapL = \frac{C V_D^2 f_s}{2} \quad (16)$$

where C=capacitance (Farad)

3. Performance Simulation

The buck/boost converter asynchronous and synchronous circuits shown in Figures 1 & 2 are modeled in Matlab/Simulink as shown in Figures 3 & 4. The analytic loss equations developed in Section 2 are modeled as shown in Figure 5 (redundant models are not shown). Figure 6 shows the simulator loss summation and efficiency calculation for the synchronous case.

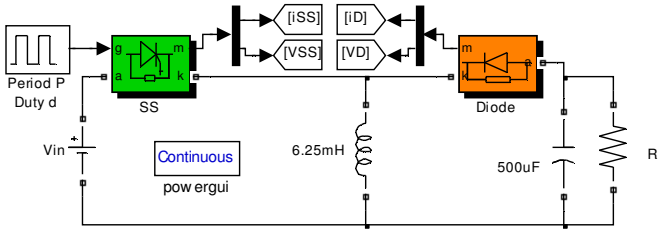

Figure 3. Buck/Boost Converter Simulation Architecture (asynchronous)

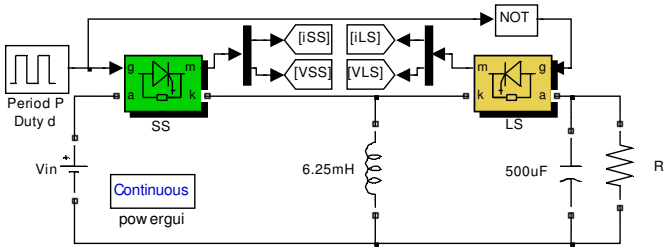

Figure 4. Buck/Boost Converter Simulation Architecture (synchronous)

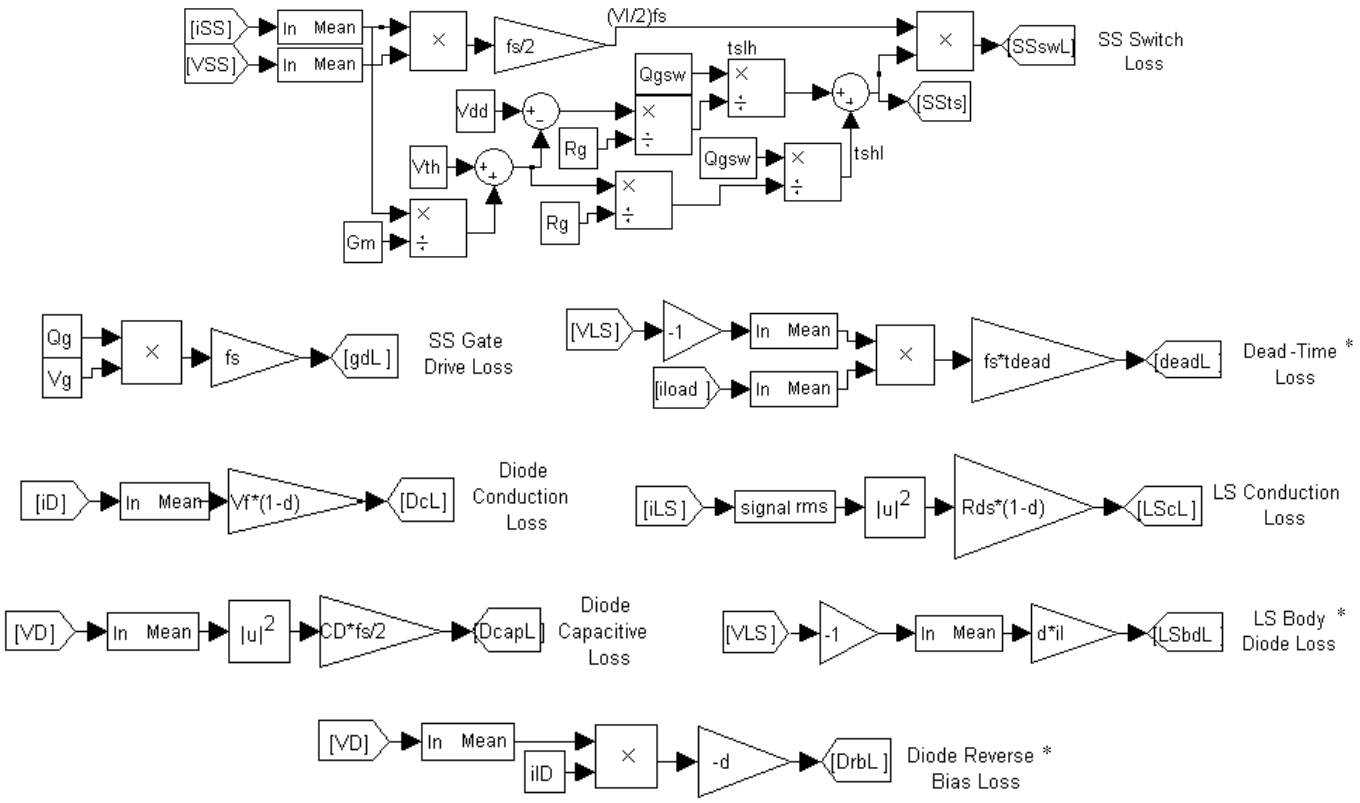

Figure 5. Simulation Loss Models

*. The (-1) factor is incidental to this simulation due to forced bias of modeling component

Both converters are evaluated at a constant Vs = Vo = 5V as this application is common for devices which require a constant supply voltage such as universal serial bus (USB) technology. Both topologies are evaluated at loads ranging from 0.01A to 1A in 10mA increments, at switching frequencies of 10kHz, 50kHz, and 100kHz. Measurements of overall efficiency are recorded for each case after stabilization of simulator transients. As a stable continuous current is usually required in loads fed by most power

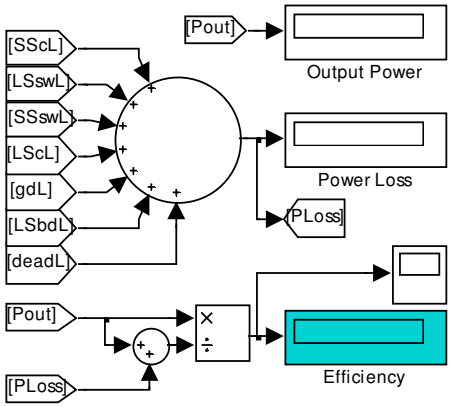

Figure 6. Simulation Loss Summation with Efficiency Calculation (synchronous)

electronic converters, only continuous conduction mode (CCM) operation is examined. The specific model MOSFET parameters used for the active switches in both converters is the IRFP450; the diode parameters used for the asynchronous converter is the SB245E.

Duty cycle is varied slightly depending on varying losses of the converter to maintain constant V_o. It is assumed that an independent voltage feedback control loop exists, independent of this work, that maintains V_o, whose losses are neglected. MOSFET controller power dissipation (resistive component of controller gate driver), resistive losses of inductor and capacitor, and reverse recovery body diode losses are also neglected.

Simulink environment simulation settings are as follows: Solver – ode45 (Dormand-Prince), Max step size – P/10, Relative tolerance – 1e-3, Min step size & Absolute tolerance – auto, simulation stop time – 10e3*P to 60e3*P depending on settling time of system (where P is switching period). The Matlab script used to support the simulation is also provided in the Appendix. One inductor size is used for all cases based on the most rigorous scenario – that with the lowest switching frequency and highest load resistance as inspection of eqn. (17) reveals, given that *d* is constant.

Table 2
Overall Buck/Boost Converter Efficiency Simulation Results

Overall Efficiency	f_s **=10kHz**		f_s **=50kHz**		f_s **=100kHz**	
i_{out} ***(mA)***	***Asynchronous***	***Synchronous***	***Asynchronous***	***Synchronous***	***Asynchronous***	***Synchronous***
10	0.89	0.914	0.7657	0.6854	0.6511	0.5212
20	0.9193	0.9512	0.8464	0.8091	0.7711	0.6819
30	0.9291	0.9654	0.8781	0.8612	0.8225	0.7579
40	0.9335	0.9714	0.8938	0.889	0.8472	0.8028
50	0.9365	0.9744	0.9037	0.9059	0.8654	0.8323
60	0.9375	0.976	0.9101	0.9174	0.8773	0.8525
70	0.9383	0.9769	0.9145	0.9257	0.8857	0.8678
80	0.9387	**0.977**[a]	0.9178	0.9315	0.8916	0.879
90	**0.939**[a]	**0.977**[a]	0.9201	0.9359	0.8967	0.8879
100	0.9389	0.9767	0.9221	0.9393	0.9009	0.8949
200	0.9351	0.9707	**0.9267**[a]	**0.9485**[a]	0.9145	0.9221
300	0.9291	0.9607	0.924	0.9443	**0.9152**[a]	**0.9245**[a]
400	0.9227	0.9502	0.9195	0.9368	0.9124	0.9207
500	0.9161	0.9397	0.9144	0.9281	0.9082	0.9139
600	0.9095	0.9292	0.9089	0.9189	0.9034	0.9063
700	0.9029	0.9189	0.9032	0.9094	0.8982	0.898
800	0.8963	0.9087	0.8974	0.8998	0.8928	0.8892
900	0.8897	0.8985	0.8916	0.8902	0.8872	0.8804
1000	0.8832	0.8886	0.8858	0.8809	0.8816	0.8716

a. Peak efficiency values shown with bold typeface

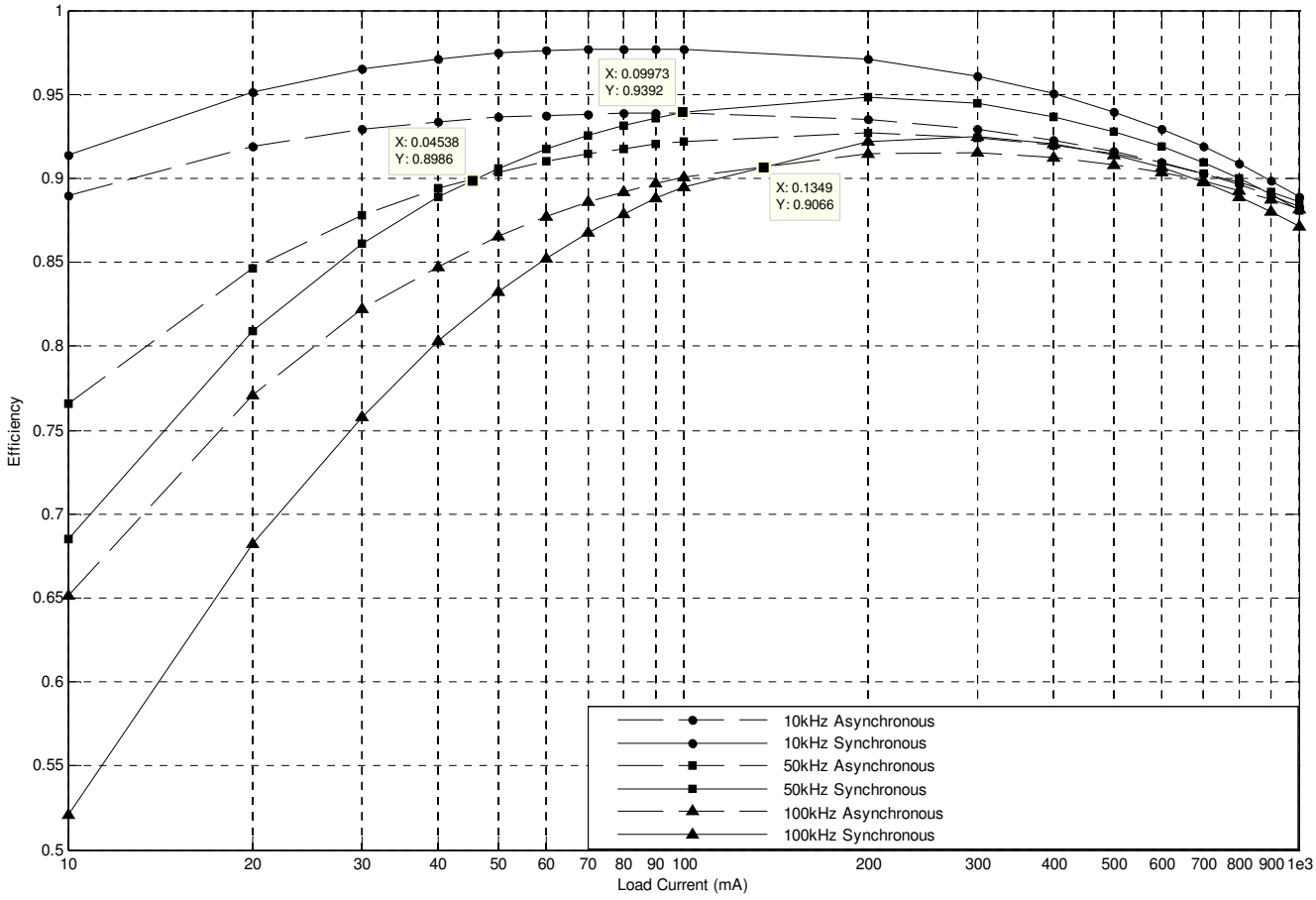

Figure 7. Overall Buck/Boost Converter Efficiency Comparison Plot – All Cases

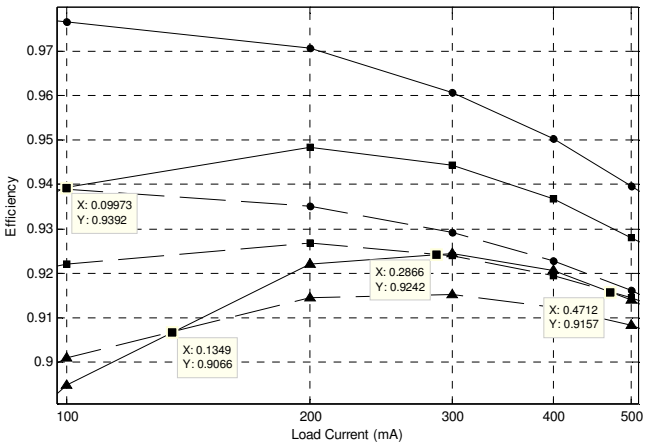

Figure 8. Detailed Overall Converter Efficiency – 100mA to 500mA Range

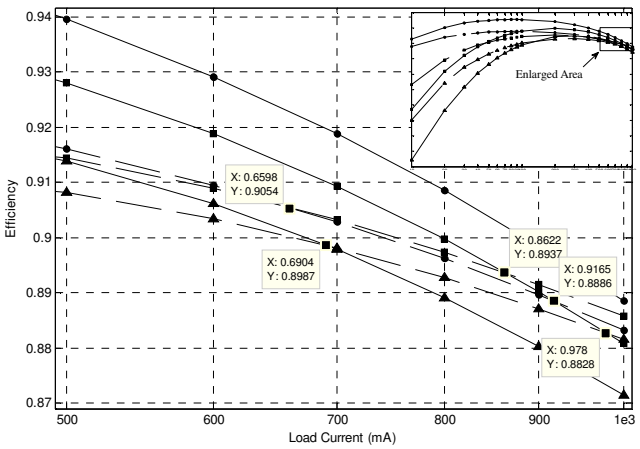

Figure 9. Detailed Overall Converter Efficiency – 500mA to 1000mA Range

$$L_{CCM_{Boundary}} = \frac{(1-d)^2\left(\frac{V_o}{I_{load}}\right)}{2f_s} = \frac{(1-0.5)^2\left(\frac{5}{0.01}\right)}{2(10e3)} = 6.25mH \quad (17)$$

Simulator efficiency and power calculation models shown in Figure 6 are based on eqns. (18) and (19), respectively.

$$Efficiency = \eta = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{P_{out}}{P_{in}} \quad (18)$$

$$P_{out} = i_{load}^2 R_{load} \quad (19)$$

4. Simulation Results

The results of recording overall efficiency for all cases are shown in Table 2 and plotted in Figures 7 - 9.

It is evident from Figure 7 that the synchronous 10kHz topology is most efficient at all loads examined, performing at a peak efficiency of 97.7% across the load range of 80 to 90mA at 5V; this configuration represents the optimal converter. Peak performance for each case is summarized in Table 3.

Table 3
Summarized Optimal Output – All Cases

Switching Frequency	*Topology*	*Efficiency*	i_{out} *(A)*
10kHz	Asynchronous	0.939	0.09
	Synchronous	0.977	0.08 - 0.09
50kHz	Asynchronous	0.927	0.2
	Synchronous	0.949	0.2
100kHz	Asynchronous	0.915	0.3
	Synchronous	0.925	0.3

Table 4
Asynchronous vs. Synchronous Optimal Load Range

Switching Frequency	*Asynchronous*	*Synchronous*	*Asynchronous*
f_s=50kHz	0-46.6mA	46.6-862mA	>862mA
f_s=100kHz	0-136mA	136-693mA	>693mA

5. Discussion

The absolute value of the slope for the synchronous converters is greater on both ends of the efficiency spectrum compared to the asynchronous, resulting in efficiency trade-off points between the two; the synchronous scenarios have a higher efficiency toward the middle section of the load range, while the asynchronous have a higher efficiency at the extremes. These points of trade-off vary between cases, summarized in Table 4. (The 10kHz case falls outside the examined range of 10mA to 1A and therefore is not included.)

The 10kHz converters have a significant advantage at light loads over the higher frequency converters as gate drive loss lowers efficiency dramatically (see appendix for loss examination).

Both synchronous and asynchronous converters are generally more efficient at lower switching frequencies. The trade-off in lowering switching frequency results in a physically larger inductor in accordance with equation (17). This may not be possible due to application size constraints, or RF interference considerations. In any case, a buck/boost converter design should incorporate the lowest switching frequency possible for loads less than 98.8mA at 5V. Loads above this point will require examination of Figures 7 - 9 for the optimal configuration.

It is noted that the results of this type of study are of course dependent on the specific electronic components chosen (see section 3 for those used in this work). Actual results will vary, but should follow the same behavior described.

6. Conclusion

MatLab/Simulink SimPower toolbox provides an effective environment for modeling and simulation of DC/DC converters. The buck/boost converter is herein optimized for efficiency considering both synchronous and asynchronous topologies with variable switching frequency and load. The optimal case offers performance at 97.7% in the load current range from 80 to 90mA at a constant 5Vin/5Vout utilizing synchronous switching at 10kHz. This configuration also proves most efficient over the entire examined load range of 10mA to 1A at 5V. In general, lower switching frequencies result in higher efficiency, particularly at light loads. All the necessary evaluation data has also been included to aid in choosing a buck/boost converter in cases where higher switching frequency than 10kHz is required, perhaps due to size limitations or electromagnetic noise generation. Output voltage and current ripple requirements may also impose design constraints.

Future work may include further exploration of loss reduction techniques in the buck/boost converter such as Zero-Voltage Switching (ZVS) [12], Mode-Hopping [11] (alternating between CCM and DCM) in cases where continuous load current is not required, and gate-drive power reduction [10]. Optimizing the converter with constant output power while modulating output voltage, current, and duty cycle may also be explored.

Appendix

Loss Details

A brief examination of losses is included here as an aid to academic understanding and potential loss reduction in future work. Individual losses from each component of the optimal converter (synchronous, f_s=10kHz) are numerically shown for consideration. Table 5 shows individual losses for the optimal converter at the extremes of the efficiency curve of Figure 7, and at the peak. Each individual loss is also given as a percentage of total loss.

Table 5
Optimal Converter Itemized Losses

	Synchronous, f_s=10kHz					
	i_{load}=10mA		**i_{load}=85mA**		**i_{load}=1000mA**	
Loss Type	***Loss (mW)***	***% of Total***	***Loss (mW)***	***% of Total***	***Loss (mW)***	***% of Total***
SSswL	2.35E-02	0.49%	0.2007	0.02%	2.453	0.39%
SScL	0.1951	4.05%	2.196	23.03%	314.7	50.20%
LSswL	2.32E-02	0.48%	0.2003	2.01%	2.393	0.38%
LScL	3.92E-02	0.82%	2.182	22.88%	299.9	47.84%
gdL	4.5	93.53%	4.5	47.20%	4.5	0.72%
LSbdL	2.50E-04	0.01%	2.50E-04	0.00%	2.53E-04	0.00%
deadL	3.00E-02	0.62%	0.2552	0.03%	2.999	0.48%

Table 6
Switching Time Ratio to Period

Switching Frequency	***Topology***	***Efficiency***	***Switch Transition (s) / Period (s)***
10kHz	Asynchronous	0.939	0.0009417
	Synchronous	0.977	0.0009411
50kHz	Asynchronous	0.927	0.00471
	Synchronous	0.949	0.004716
100kHz	Asynchronous	0.915	0.009456
	Synchronous	0.925	0.009448

Table 5 reveals that gate drive losses lead the optimal case (i_{load}=*85mA)* at 47%, followed by conduction losses at 46%. At i_{load} = 1A the converter is dominated by conduction losses at 98%.

Losses that are a function of switching frequency are: MOSFET switching loss, gate drive loss, and dead time loss for the synchronous case, while only diode capacitive loss affects the asynchronous case. Since diode capacitive loss is relatively small in comparison to the sum of the synchronous losses associated with the addition of the load MOSFET, the asynchronous converter performs better at the higher switching frequencies with lighter loads. As expected then, the worst performer at light loads is the 100kHz synchronous converter due to high losses associated with switching as shown in Table 5 and Figure 7. Examination of equation (10) shows gate drive loss is a function only of switching frequency, and therefore dominates at light loads. This makes intuitive sense considering that a certain minimum amount of energy is required to operate the switches, and compare that amount to relatively low overall output energy.

The switching loss equation (9) shows that losses occur during the time that the voltage across a switch and current through it are transitioning from off to on and vice-versa. The switching time ratio to period calculation is therefore an effective tool in understanding the percentage of each period that switching losses are incurred (Figure 10). The portion of each period in which the transistors take to complete their transition is calculated at the peak of each converter's efficiency as shown in Table 6.

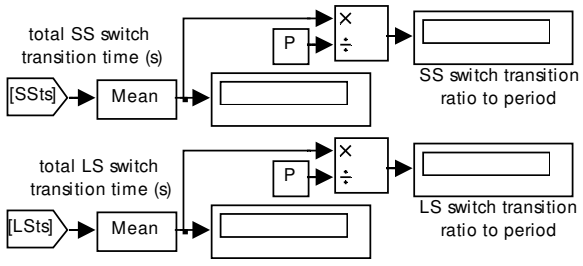

Figure 10. Switching Time Ratio to Period Calculation

Table 6 shows that it takes approximately 1% of the switching period at 100kHz for the converter switches to complete the switching operation, or 0.1 µs.

Matlab Workspace Simulation Supporting Code

```
%% The Buck Boost Converter
%IRFP450 MOSFET Data Sheet Parameters
Rds=0.33; %Ohm - Drain to Source ON
resistance
Qg=75e-9; %Coulomb - FET gate charge
Qgs=13.5e-9; %Coulomb - FET gate-source
charge
Rg=4.7; %Ohm - FET gate resistance
Vg=3.0; %Volt - gate drive voltage
il=100e-9; %Amp - body diode leakage current
Gm=10; %Siemens - transconductance

%SB245E Diode Data Sheet Parameters
Vf=0.5; %Volt - Diode forward voltage
ilD=0.5e-3; %Amp - typical diode leakage
current
CD=170e-12; %Farad - diode terminal
capacitance

%Evaluation Parameters
Vdd=5.0; %Volt - driver circuit typical
design voltage (input Vs)
Vin=5; %Volt - Input Voltage Signal to
Buck/Boost
fs=100e3; %1/Second - switching frequency
P=1/fs; %Second - switching period
Vout=5; %Volt - desired output voltage
d=(Vin/(Vin+Vout))*1.055; %unitless ratio -
duty calculation with scaling factor for
losses
I=0.8; %Amp - desired load current
R=Vout/I; %Ohm - calculation of load
resistance
Lccm=(((1-d)^2*R)/(2*(1/P))); %Henry -
minimum L value for CCM
Qgsw=24e-9; %Coulomb - gate threshold charge
per Xiong et. al. [5] (Former Qg+(Qgs/2) per
Klein)
tdead=60e-9; %Second - typical according to
Djekic [2] page 1375
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